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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,742	03/12/2004	Richard Parent	CD03011	9219
7590	10/31/2005		EXAMINER MAI, SON LUU	
Bradley T. Sako WALKER & SAKO, LLP Suite 235 300 South First Street San Jose, CA 95113			ART UNIT	PAPER NUMBER
			2827	
			DATE MAILED: 10/31/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

<b>Office Action Summary</b>	<b>Application No.</b> 10/799,742	<b>Applicant(s)</b> PARENT ET AL.	
	<b>Examiner</b> Son L. Mai	<b>Art Unit</b> 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 12-20 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-8 and 14-20 is/are allowed.
- 6) ☒ Claim(s) 9, 10, 12 and 13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. The papers filed 08-08-05 has been entered. Accordingly claims 1-10 and 12-20 are pending.

#### ***Claim Objections***

2. Claim 9 is objected to because of the following informalities: In line 5, "the conductive line" should read --a conductive line of the plurality of conductive lines--. Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Furutani (U.S. Patent 5,673,231).

Regarding claim 9, Furutani teaches a method of reducing a standby current contribution in conductive lines of a memory device, comprising the steps of: providing at least one transistor (transistor 21 in figure 1) between each of a plurality of conductive lines (BL0a) arranged in a first direction within a memory cell array and a corresponding circuit (amplifier 5) coupled to a conductive line (I/O line); including providing at least one transistor between a bitline (BL0a) and a corresponding sense amplifier circuit; programming a fuse-type element (fuse 12) to generate a control signal first value (signal Y0 is brought to low level) if an associated conductive line is

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determined to have a defect, and disabling each transistor when the associated control signal has the first value to prevent defect induced current from flowing through the transistor with respect to the corresponding conductive line (see column 9, line 65 through column 10, line 33).

Regarding claim 12, even though not shown in figure 1, an equalization circuit is included in the sense amplifier circuit 5 as a means to equalize the data line pair I/O before reading data from memory array cells.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furutani (U.S. Patent 5,673,231) as applied to claim 9 above, and further in view of Yamauchi et al. (U.S. Patent 6,246,627).

Furutani teaches all the limitations of independent claim 9 except for the limitation of claim 10 wherein the step of programming the fuse-type element is performed in a wafer test procedure. Yamauchi, from the same field of endeavor, teaches at column 1, lines 38-64, that the step of programming is known. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to program the fuse-type element in a wafer test procedure, because it would be easy to

perform programming at the final stage of the fabrication process and would improve the production yield.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furutani (U.S. Patent 5,671,231) as applied to claim 9 above, and further in view of Kawai et al. (U.S. Patent 5,146,429).

Furutani teaches all the limitations of independent claim 9 except for the limitation of claim 13 wherein the step of providing at least one transistor includes providing at least one transistor between a wordline and a corresponding wordline driver circuit. Kawai, from the same field of endeavor, teaches in figure 5, one transistor (transistor N) is positioned between a wordline (R1) and a corresponding wordline driver circuit (ROW DECODER 3). This is to connect or disconnect the wordline and driver circuit when the wordline is normal or defective. Therefore it would have been obvious to one of ordinary skill in the art to apply Kawai's teaching to Furutani's disclosure to further isolate defective wordlines from wordline driver circuits and reduce power consumption in standby mode.

***Allowable Subject Matter***

8. Claims 1-8,14-20 are allowed.

***Response to Arguments***

9. Applicant's arguments filed 08-08-05 have been fully considered but they are not persuasive. In the Remarks, the Applicants argued that the Furutani patent teaches away from claim 9 of the instant application and cited some paragraphs of Furutani to support the arguments. The cited paragraphs, however, are not the only disclosure of

Furutani's invention. As pointing out in the preceding rejections, Furutani clearly discloses at column 9, line 65 through column 10, line 33, the step of disabling each transistor when the associated control signal has the first value to prevent defect induced current from flowing through the transistor with respect to the corresponding conductive line.

### ***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10-26-05



Son L. Mai  
Primary Examiner  
Art Unit 2827